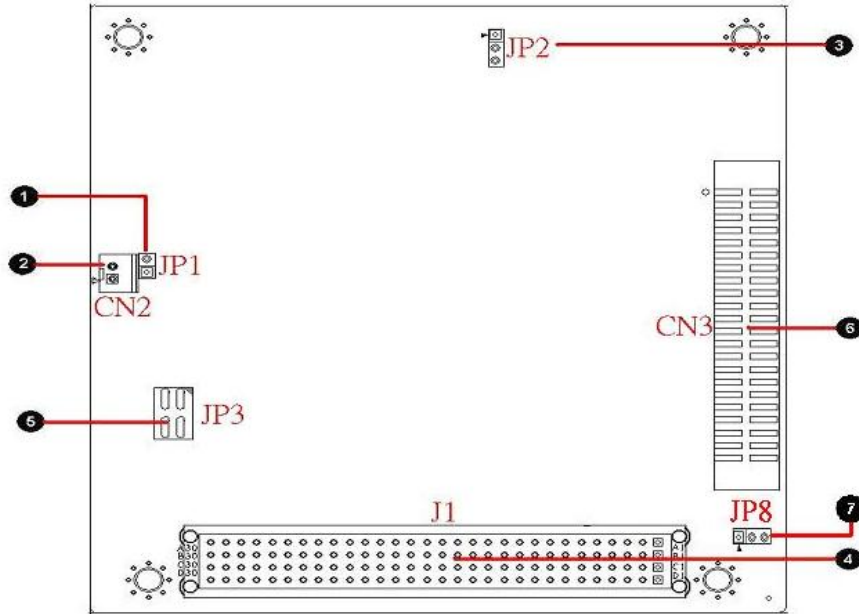





AR-B104D Quick Manual V1.0

1. Mainboard illustration (Top Side)



1 JP1 CAN Bus terminal resister select pin header.	4 J1 PCI BUS connector (PC-104 Plus)
2 CN2 CAN Bus connector	5 JP3 Operation mode selection.
3 JP2 Clear SRAM pin header.	6 CN3 GPIO connector.
7 JP8 SRAM mode select.	

2. Connector and Jumper Setting Table

1. JP1		2. CN2		3. JP2																			
 1	<table border="1"> <thead> <tr> <th>Pin</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>close</td> <td>120 ohm resister.</td> </tr> <tr> <td>open</td> <td>None.</td> </tr> </tbody> </table>	Pin	Description	close	120 ohm resister.	open	None.	 1 2	<table border="1"> <thead> <tr> <th>Pin</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>CAN High</td> </tr> <tr> <td>2</td> <td>CAN Low</td> </tr> </tbody> </table>	Pin	Description	1	CAN High	2	CAN Low	 1 2 3	<table border="1"> <thead> <tr> <th>Pin</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>1-2</td> <td>Normal</td> </tr> <tr> <td>2-3</td> <td>Clear SRAM</td> </tr> </tbody> </table>	Pin	Description	1-2	Normal	2-3	Clear SRAM
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1-2	Normal																						
2-3	Clear SRAM																						

4. CN4

PIN	define	PIN	define	PIN	define	PIN	define	PIN	define	PIN	define	PIN	define	PIN	define
A1	GND	B1	SIRQ	A16	AD21	B16	AD20	C1	+5V	D1	AD00	C16	GND	D16	AD19
A2	VIO	B2	AD02	A17	3.3V	B17	AD23	C2	AD01	D2	+5V	C17	AD22	D17	+3.3V
A3	AD05	B3	GND	A18	IDSEL0	B18	GND	C3	AD04	D3	AD03	C18	IDSEL1	D18	IDSEL2
A4	CBE0#	B4	AD07	A19	AD24	B19	CBE3#	C4	GND	D4	AD06	C19	VIO	D19	IDSEL3
A5	GND	B5	AD09	A20	GND	B20	AD26	C5	AD08	D5	GND	C20	AD25	D20	GND
A6	AD11	B6	VIO	A21	AD29	B21	+5V	C6	AD10	D6	M66EN	C21	AD28	D21	AD22
A7	AD14	B7	AD13	A22	+5V	B22	AD30	C7	GND	D7	AD12	C22	GND	D22	AD31
A8	3.3V	B8	CBE1#	A23	REQ0#	B23	GND	C8	AD15	D8	+3.3V	C23	REQ1#	D23	VIO
A9	SERR#	B9	GND	A24	GND	B24	REQ2#	C9	SB0	D9	PAR	C24	+5V	D24	GNT0#
A10	GND	B10	PERR#	A25	GNT1#	B25	VIO	C10	+3.3V	D10	SDONE	C25	GNT2#	D25	GND
A11	STOP#	B11	+3.3V	A26	+5V	B26	PCICLK0	C11	LOCK#	D11	GND	C26	GND	D26	PCICLK1
A12	3.3V	B12	TRDY#	A27	PCICLK2	B27	+5V	C12	GND	D12	DEVDEL#	C27	PCICLK3	D27	GND
A13	FRAME#	B13	GND	A28	GND	B28	INTD#	C13	IRDY#	D13	+3.3V	C28	+5V	D28	RST#
A14	GND	B14	AD16	A29	+12V	B29	INTA#	C14	+3.3V	D14	CBE2#	C29	INTB#	D29	INTC#
A15	AD18	B15	+3.3V	A30	-12V	B30	REQ3#	C15	AD17	D15	GND	C30	GNT3#	D30	GND

5. JP3



Pin	Description
1-2,3-4 open	Mode 3
1-2 open,3-4 short	Mode 2
1-2 short,3-4 open	Mode 1
1-2,3-4 short	Mode 0

Note: The JP3 default setting is Mode0.

• Operation mode description

	PCICLK	IDSEL	INT 0
Mode 0	PCICLK0	IDSEL0	A
Mode 1	PCICLK1	IDSEL1	B
Mode 2	PCICLK2	IDSEL2	C
Mode 3	PCICLK3	IDSEL3	D

6. CN3



PIN	DESCRIPTION	PIN	DESCRIPTION
1	GPI0	2	GPI1
3	GPI2	4	GPI3
5	GPI4	6	GPI5
7	GPI6	8	GPI7
9	GPI8	10	GPI9
11	GPI10	12	GPI11
13	GND	14	GND
15	GND	16	GND
17	GND	18	GND
19	GND	20	GND
21	GND	22	GND
23	GPO0	24	GPO1
25	GND	26	GND
27	GPO2	28	GPO3
29	GND	30	GND
31	GPO4	32	GPO5
33	GND	34	GND
35	GPO6	36	GPO7
37	GND	38	GND
39	GPO8	40	GPO9
41	GND	42	GND
43	GPO10	44	GPO11

7. JP8



Pin	Description
1-2	Memory mode
open	Disk mode