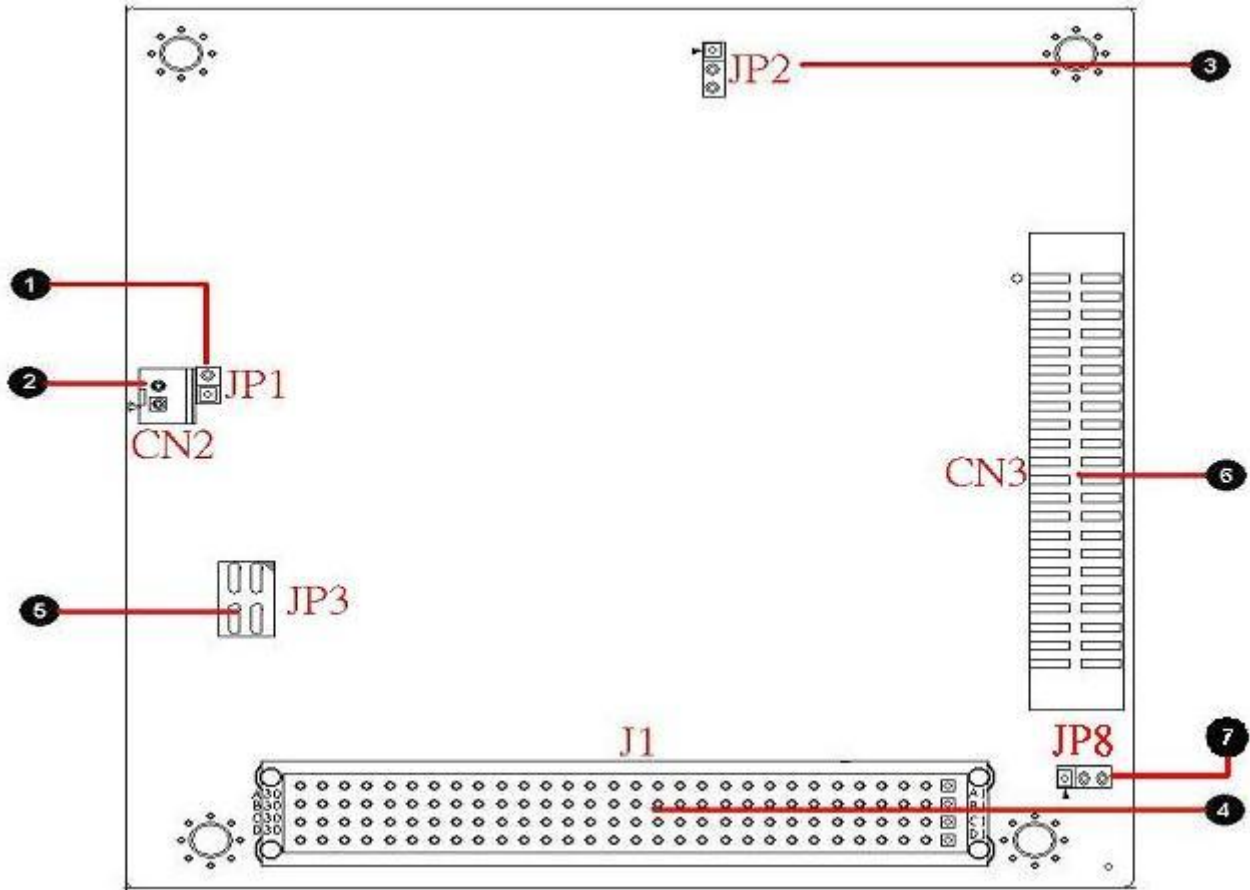





# AR-B104D Quick Manual V1.01

## 1. Mainboard illustration (Top Side)



①	<b>JP1</b> CAN Bus terminal resistor select pin header.	④	<b>J1</b> PCI BUS connector (PC-104 Plus)
②	<b>CN2</b> CAN Bus connector	⑤	<b>JP3</b> Operation mode selection.
③	<b>JP2</b> Clear SRAM pin header.	⑥	<b>CN3</b> GPIO connector.
⑦	<b>JP8</b> SRAM mode select.		

## 2.Connector and Jumper Setting Table

1. JP1		2. CN2		3. JP2																			
 1	<table border="1"> <thead> <tr> <th>Pin</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>close</td> <td>120 ohm resistor.</td> </tr> <tr> <td>open</td> <td>None.</td> </tr> </tbody> </table>	Pin	Description	close	120 ohm resistor.	open	None.	 1 2	<table border="1"> <thead> <tr> <th>Pin</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>CAN High</td> </tr> <tr> <td>2</td> <td>CAN Low</td> </tr> </tbody> </table>	Pin	Description	1	CAN High	2	CAN Low	 1 2 3	<table border="1"> <thead> <tr> <th>Pin</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>1-2</td> <td>Normal</td> </tr> <tr> <td>2-3</td> <td>Clear SRAM</td> </tr> </tbody> </table>	Pin	Description	1-2	Normal	2-3	Clear SRAM
Pin	Description																						
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2-3	Clear SRAM																						

### 4. CN4

PIN	define	PIN	define	PIN	define	PIN	define	PIN	define	PIN	define	PIN	define	PIN	define
A1	GND	B1	SIRQ	A16	AD21	B16	AD20	C1	+5V	D1	AD00	C16	GND	D16	AD19
A2	VIO	B2	AD02	A17	3.3V	B17	AD23	C2	AD01	D2	+5V	C17	AD22	D17	+3.3V
A3	AD05	B3	GND	A18	IDSEL0	B18	GND	C3	AD04	D3	AD03	C18	IDSEL1	D18	IDSEL2
A4	CBE0#	B4	AD07	A19	AD24	B19	CBE3#	C4	GND	D4	AD06	C19	VIO	D19	IDSEL3
A5	GND	B5	AD09	A20	GND	B20	AD26	C5	AD08	D5	GND	C20	AD25	D20	GND
A6	AD11	B6	VIO	A21	AD29	B21	+5V	C6	AD10	D6	M66EN	C21	AD28	D21	AD22
A7	AD14	B7	AD13	A22	+5V	B22	AD30	C7	GND	D7	AD12	C22	GND	D22	AD31
A8	3.3V	B8	CBE1#	A23	REQ0#	B23	GND	C8	AD15	D8	+3.3V	C23	REQ1#	D23	VIO
A9	SERR#	B9	GND	A24	GND	B24	REQ2#	C9	SB0	D9	PAR	C24	+5V	D24	GNT0#
A10	GND	B10	PERR#	A25	GNT1#	B25	VIO	C10	+3.3V	D10	SDONE	C25	GNT2#	D25	GND
A11	STOP#	B11	+3.3V	A26	+5V	B26	PCICLK0	C11	LOCK#	D11	GND	C26	GND	D26	PCICLK1
A12	3.3V	B12	TRDY#	A27	PCICLK2	B27	+5V	C12	GND	D12	DEVDEL#	C27	PCICLK3	D27	GND
A13	FRAME#	B13	GND	A28	GND	B28	INTD#	C13	IRDY#	D13	+3.3V	C28	+5V	D28	RST#
A14	GND	B14	AD16	A29	+12V	B29	INTA#	C14	+3.3V	D14	CBE2#	C29	INTB#	D29	INTC#
A15	AD18	B15	+3.3V	A30	-12V	B30	REQ3#	C15	AD17	D15	GND	C30	GNT3#	D30	GND

5. JP3



Pin	Description
1-2,3-4 open	<b>Mode 3</b>
1-2 open,3-4 short	<b>Mode 2</b>
1-2 short,3-4 open	<b>Mode 1</b>
1-2,3-4 short	<b>Mode 0</b>

**Note:** The JP3 default setting is Mode0.

• Operation mode description

	PCICLK	IDSEL	INT 0
<b>Mode 0</b>	PCICLK0	IDSEL0	A
<b>Mode 1</b>	PCICLK1	IDSEL1	B
<b>Mode 2</b>	PCICLK2	IDSEL2	C
<b>Mode 3</b>	PCICLK3	IDSEL3	D

**6. CN3**



PIN	DESCRIPTION	PIN	DESCRIPTION
1	GPI0	2	GPI1
3	GPI2	4	GPI3
5	GPI4	6	GPI5
7	GPI6	8	GPI7
9	GPI8	10	GPI9
11	GPI10	12	GPI11
13	GND	14	GND
15	GND	16	GND
17	GND	18	GND
19	GND	20	GND
21	GND	22	GND
23	GPO0	24	GPO1
25	GND	26	GND
27	GPO2	28	GPO3
29	GND	30	GND
31	GPO4	32	GPO5
33	GND	34	GND
35	GPO6	36	GPO7
37	GND	38	GND
39	GPO8	40	GPO9
41	GND	42	GND
43	GPO10	44	GPO11

**7. JP8**



Pin	Description
1-2	Memory mode
open	Disk mode

## 3.AR-B104D digital I/O, SRAM disk & CAN bus Module

AR-B104D is a PCI-104 super I/O module which equipped with CAN bus, SRAM disk and digital I/Os on a single module.

### Features

- 1x 2KV isolated CAN bus. Support 2.0A and 2.0B protocol.
- Time stamp of CAN message
- 1MB battery backup SRAM disk. Supports disk and memory modes.
- 12x optical isolated digital inputs. Support counter mode.
- 12x 500 mA current sink digital outputs. Support pulse generator mode.
- Linux and Windows 2000, XP Software Development Kit (SDK).

### Specifications

General	
Bus interface	<ol style="list-style-type: none"> <li>1. PCI 104</li> <li>2. PCI 2.0 Compliant</li> </ol>
SRAM disk	<ol style="list-style-type: none"> <li>1. Capacity: 1M Bytes</li> <li>2. Battery backup</li> <li>3. Operation mode:                             <ol style="list-style-type: none"> <li>A. Memory Mode</li> <li>B. Disk Mode</li> <li>C. Mode selection through Jumper (factory default disk mode)</li> </ol> </li> </ol>
Digital Input	<ol style="list-style-type: none"> <li>1. 12 optical isolated channels</li> <li>2. Operating mode:                             <ol style="list-style-type: none"> <li>A. General digital input</li> <li>B. Counter mode</li> </ol> </li> <li>3. Programmable de-bounce time (0 ms to 255ms, 1 ms resolution).</li> <li>4. Support Change of State interrupt</li> <li>5. Response time: 20 uS + de-bounce time</li> <li>6. Response time: OPTO (delay time + OPTO rising time = 20uS) + debounce time. Default = 16.02ms.</li> <li>7. Trigger: rising trigger or falling trigger</li> <li>8. Signal Type:                             <ol style="list-style-type: none"> <li>A. Open/Ground switch input</li> </ol> </li> </ol>

	<ul style="list-style-type: none"> <li>B. Digital Logic                             <ul style="list-style-type: none"> <li>i. Logic High: 3V to 28V</li> <li>ii. Logic Low: 0V to 1.5V</li> </ul> </li> <li>9. Maximum input frequency 10KHz( duty = 50% ).</li> </ul>	
Counter	<ul style="list-style-type: none"> <li>1. All digital input support counter mode</li> <li>2. 12 x independent 16-bit counters</li> <li>3. Connect to all digital inputs</li> <li>4. Operation Mode:                             <ul style="list-style-type: none"> <li>a. Count to number interrupt.</li> <li>b. Read and clear</li> <li>c. Read on the fly</li> <li>d. Auto stop counting after programmable constant state interval(Interrupt active after programmable constant state interval Resolution: 1ms, and 100ms)</li> </ul> </li> </ul>	
Digital Output	<ul style="list-style-type: none"> <li>1. 12 channels</li> <li>2. Output Type: Open drain MOSFET driver</li> <li>3. Output voltage range: 5V to 30V</li> <li>4. Sink Current: maximum 500mA each channel</li> <li>5. Power on initial state: MOSFET off</li> <li>6. Support pulse generator                             <ul style="list-style-type: none"> <li>A. Programmable cycle time, duty cycle and number of cycles. User defines on and off periods (maximum 8-bit for on and off period value).</li> <li>B. Maximum 65535 cycles</li> <li>C. RUN &amp; STOP command</li> <li>D. Programmable time unit: 1 ms, 100ms and 1 second</li> </ul> </li> </ul>	
Timer	<ul style="list-style-type: none"> <li>1. 12 x independent 16-bit timers</li> <li>2. Support Time Out Interrupt</li> <li>3. Programmable time unit: 1 ms and 100ms</li> </ul>	
CAN bus	<ul style="list-style-type: none"> <li>1. 1 x CAN bus</li> <li>2. 2KV isolation</li> <li>3. Support both CAN 2.0A and 2.0B protocol</li> <li>4. Programmable baud rate: from 5K bps Maximum 1M bps or user-defined baud rate</li> <li>5. Time stamp of CAN message</li> </ul>	

	6. API library for user development 7. CAN bus device status query 8. Device driver for Windows 2000/XP/XPe and Linux	
Maximum card	Maximum 2 cards can be stacked up in one system	
Software	1. Windows XP, XPe and Linux device driver and API 2. Windows XP, XPe and Linux demo program 3. User interface for DIO, SRAM and CAN bus in Linux and Windows XP embedded	
<b>Mechanical</b>		
Dimension	90.17 x 95.89mm (3.55"x3.775")	
Operating Temp.	-20°C to 70°C (-1~158°F) without air flow	
Storage Temp.	-20~85°C (-4~185°F)	
Relative Humidity	0 to 90% @ 40°C, non-condensing (95% @ 40°C, Non-Condensing by request)	
<b>EMC &amp; Safety</b>		
EMC	CE, FCC	