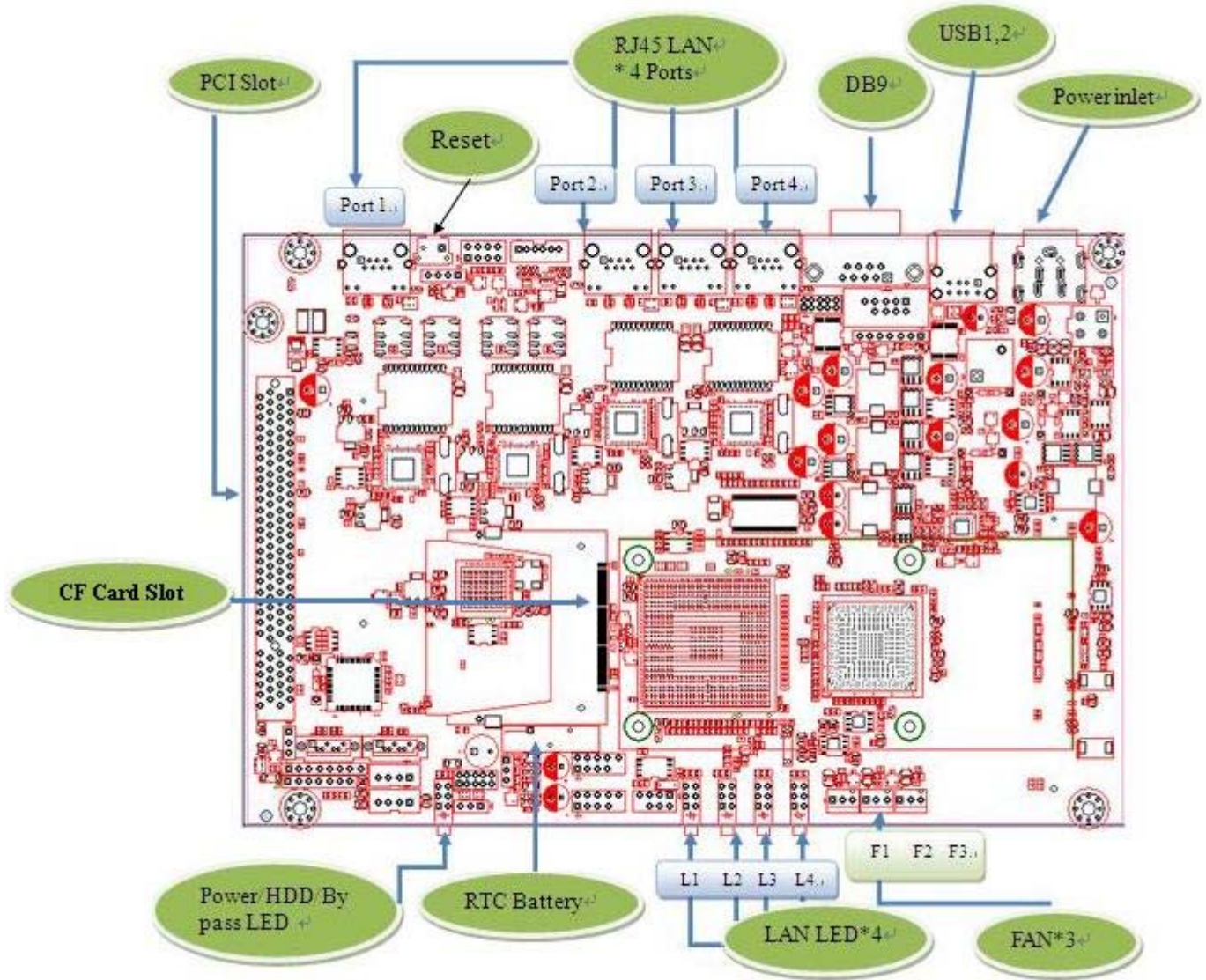
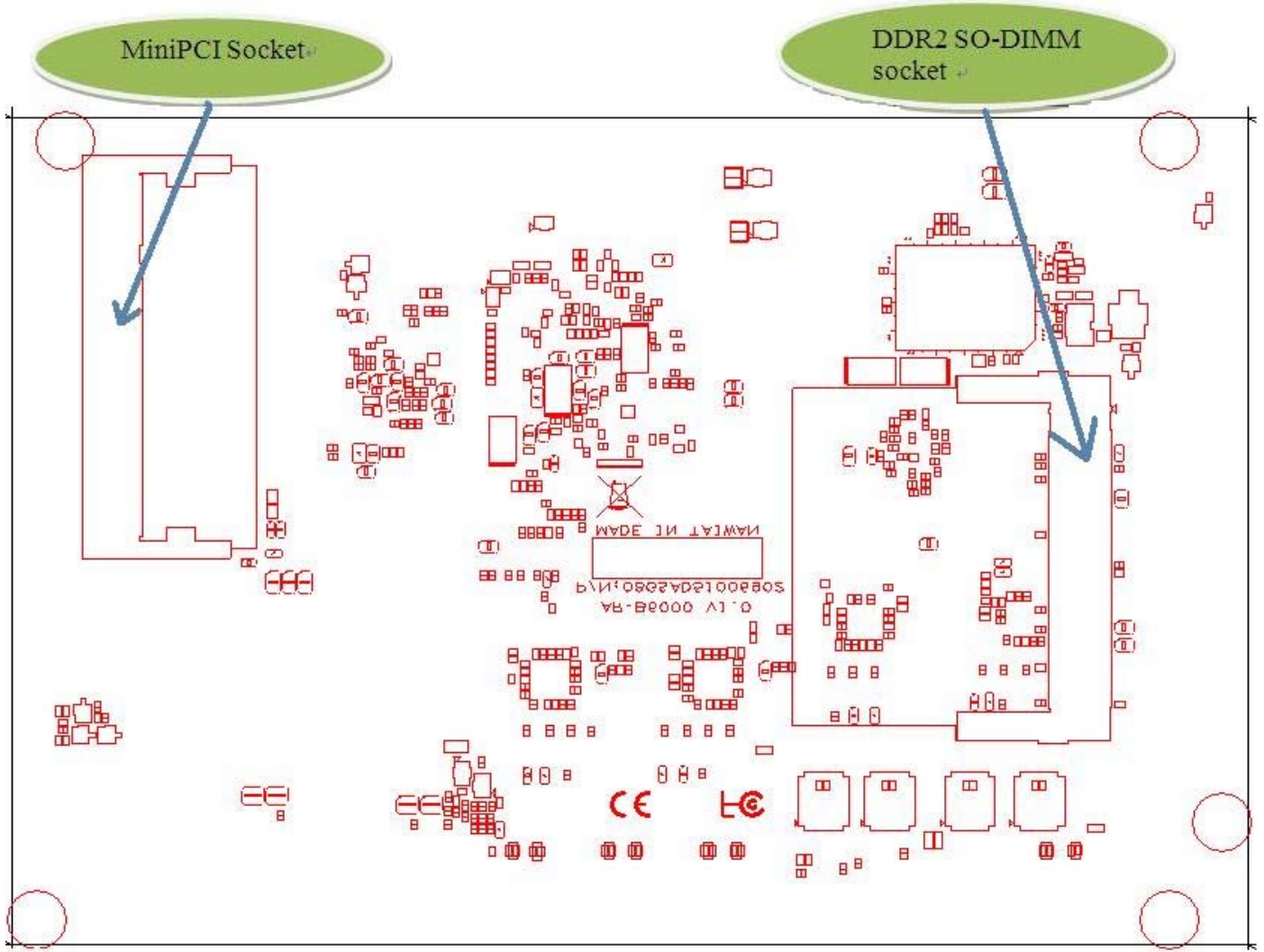


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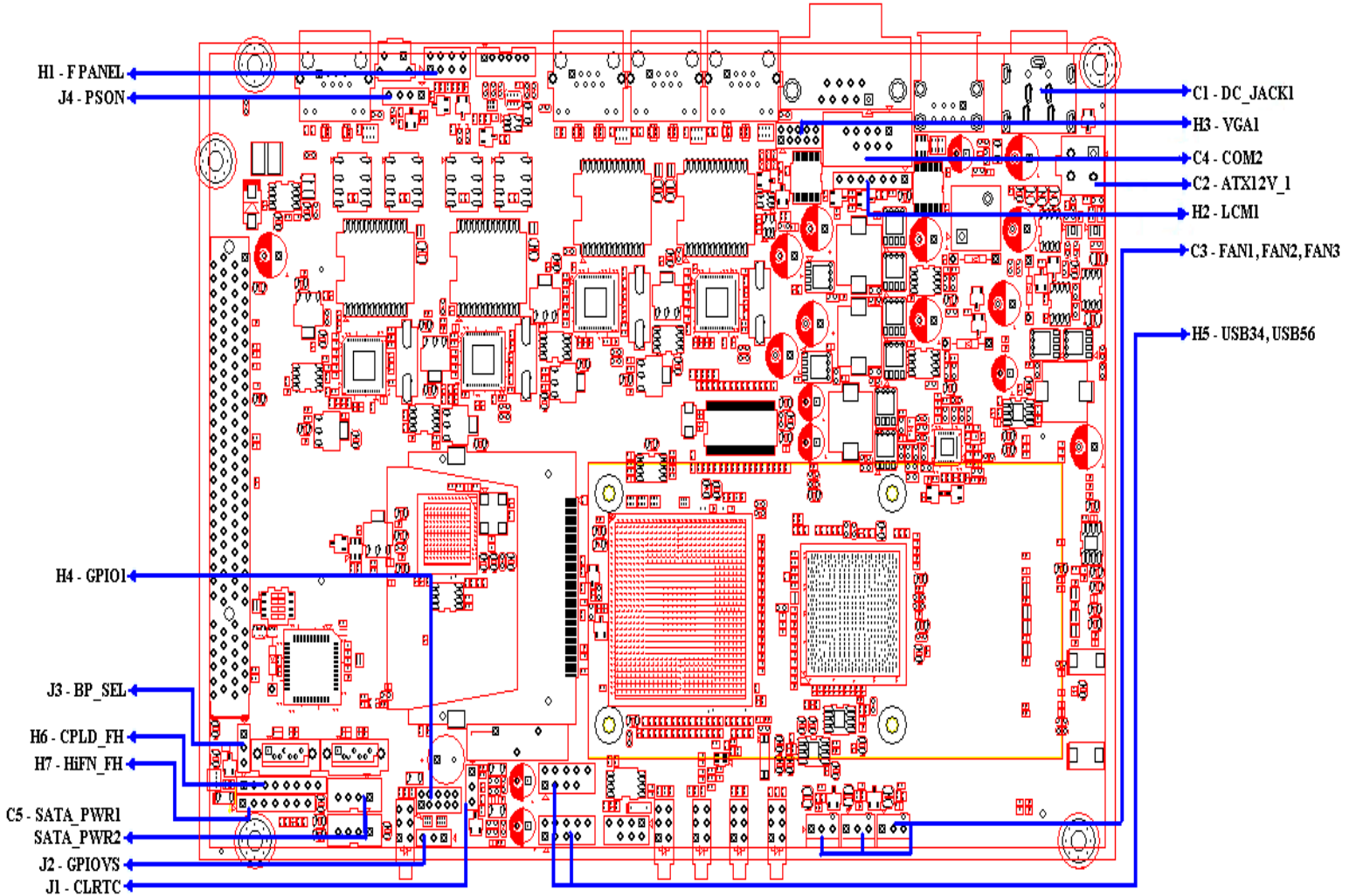
1. Mainboard illustration (Top Side)






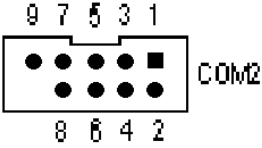
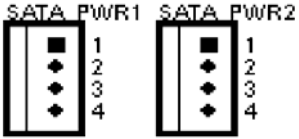
1.1 Mainboard illustration (Bottom Side)



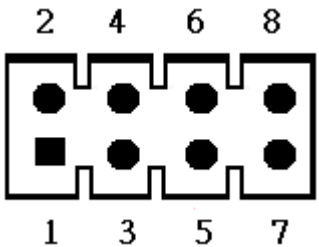

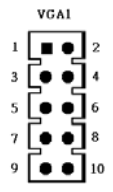
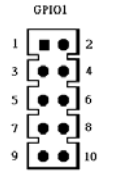
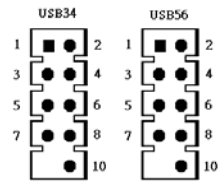
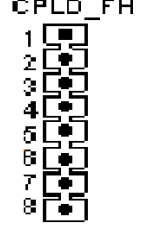
2. Locations of IO ports & Jumper settings definition







2.1 Pin definition for Connector

Item	Connector NAME	DESCRIPTION																								
C1	DC_JACK1 	Power Inlet Power connector for Adapter POWER-IN <table border="1" data-bbox="1019 430 1243 519"> <thead> <tr> <th>PIN</th> <th>SIGNAL</th> </tr> </thead> <tbody> <tr> <td>Up Side</td> <td>12V</td> </tr> <tr> <td>Bottom side</td> <td>GND</td> </tr> </tbody> </table>	PIN	SIGNAL	Up Side	12V	Bottom side	GND																		
PIN	SIGNAL																									
Up Side	12V																									
Bottom side	GND																									
C2	ATX12V_1 	Power input (CO lay with Power inlet) Connector for Regular ATX 4 pin 12V Input <table border="1" data-bbox="995 633 1219 723"> <thead> <tr> <th>PIN</th> <th>SIGNAL</th> </tr> </thead> <tbody> <tr> <td>Right Side</td> <td>12V</td> </tr> <tr> <td>Left Side</td> <td>GND</td> </tr> </tbody> </table>	PIN	SIGNAL	Right Side	12V	Left Side	GND																		
PIN	SIGNAL																									
Right Side	12V																									
Left Side	GND																									
C3	FAN1 , FAN2, FAN3 	FAN connector*3 (for CPU FAN*1, System FAN*2) <table border="1" data-bbox="927 777 1257 904"> <thead> <tr> <th>PIN</th> <th>Signal</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>GND</td> </tr> <tr> <td>2</td> <td>+12V</td> </tr> <tr> <td>3</td> <td>SENSE</td> </tr> </tbody> </table>	PIN	Signal	1	GND	2	+12V	3	SENSE																
PIN	Signal																									
1	GND																									
2	+12V																									
3	SENSE																									
C4	COM2 	<table border="1" data-bbox="871 927 1323 1093"> <thead> <tr> <th>Pin</th> <th>Signal</th> <th>Pin</th> <th>Signal</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>/DCD</td> <td>2</td> <td>/DSR</td> </tr> <tr> <td>3</td> <td>RX</td> <td>4</td> <td>/RTS</td> </tr> <tr> <td>5</td> <td>TX</td> <td>6</td> <td>/CTS</td> </tr> <tr> <td>7</td> <td>/DTR</td> <td>8</td> <td>/RI</td> </tr> <tr> <td>9</td> <td>GND</td> <td>10</td> <td>N.C.</td> </tr> </tbody> </table>	Pin	Signal	Pin	Signal	1	/DCD	2	/DSR	3	RX	4	/RTS	5	TX	6	/CTS	7	/DTR	8	/RI	9	GND	10	N.C.
Pin	Signal	Pin	Signal																							
1	/DCD	2	/DSR																							
3	RX	4	/RTS																							
5	TX	6	/CTS																							
7	/DTR	8	/RI																							
9	GND	10	N.C.																							
C5	SATA_PWR1,SATA_PWR2 	<table border="1" data-bbox="820 1122 1370 1330"> <thead> <tr> <th>Pin↴</th> <th>Description↴</th> </tr> </thead> <tbody> <tr> <td>1↴</td> <td>+V5↴</td> </tr> <tr> <td>2↴</td> <td>GND↴</td> </tr> <tr> <td>3↴</td> <td>+V3.3↴</td> </tr> <tr> <td>4↴</td> <td>+V12↴</td> </tr> </tbody> </table>	Pin↴	Description↴	1↴	+V5↴	2↴	GND↴	3↴	+V3.3↴	4↴	+V12↴														
Pin↴	Description↴																									
1↴	+V5↴																									
2↴	GND↴																									
3↴	+V3.3↴																									
4↴	+V12↴																									

2.2 Pin definition for Header

Item	HEADER NAME	DESCRIPTION																								
H1	<p>F_PANEL</p> 	<p>Panel Connector (2*4pin, 2.54mm)</p> <table border="1"> <thead> <tr> <th>Pin</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>1-2</td> <td>HDD Active LED</td> </tr> <tr> <td>3-4</td> <td>Power on LED</td> </tr> <tr> <td>5-6</td> <td>Bypass Active LED</td> </tr> <tr> <td>7-8</td> <td>Reset</td> </tr> </tbody> </table>	Pin	Description	1-2	HDD Active LED	3-4	Power on LED	5-6	Bypass Active LED	7-8	Reset														
Pin	Description																									
1-2	HDD Active LED																									
3-4	Power on LED																									
5-6	Bypass Active LED																									
7-8	Reset																									
H2	<p>LCM1</p> 	<table border="1"> <thead> <tr> <th>PIN</th> <th>SIGNAL</th> <th>PIN</th> <th>SIGNAL</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>Level high</td> <td>2</td> <td>+5V</td> </tr> <tr> <td>3</td> <td>TXDB</td> <td>4</td> <td>RXDB</td> </tr> <tr> <td>5</td> <td>/RTSB</td> <td>6</td> <td>/CTSB</td> </tr> <tr> <td>7</td> <td>GND</td> <td></td> <td></td> </tr> </tbody> </table>	PIN	SIGNAL	PIN	SIGNAL	1	Level high	2	+5V	3	TXDB	4	RXDB	5	/RTSB	6	/CTSB	7	GND						
PIN	SIGNAL	PIN	SIGNAL																							
1	Level high	2	+5V																							
3	TXDB	4	RXDB																							
5	/RTSB	6	/CTSB																							
7	GND																									
H3	<p>VGA1</p> 	<table border="1"> <thead> <tr> <th>PIN</th> <th>Signal</th> <th>PIN</th> <th>Signal</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>RED</td> <td>2</td> <td>GND</td> </tr> <tr> <td>3</td> <td>GREEN</td> <td>4</td> <td>GND</td> </tr> <tr> <td>5</td> <td>BLUE</td> <td>6</td> <td>GND</td> </tr> <tr> <td>7</td> <td>VSYNC</td> <td>8</td> <td>SCL</td> </tr> <tr> <td>9</td> <td>HSYNC</td> <td>10</td> <td>SDA</td> </tr> </tbody> </table>	PIN	Signal	PIN	Signal	1	RED	2	GND	3	GREEN	4	GND	5	BLUE	6	GND	7	VSYNC	8	SCL	9	HSYNC	10	SDA
PIN	Signal	PIN	Signal																							
1	RED	2	GND																							
3	GREEN	4	GND																							
5	BLUE	6	GND																							
7	VSYNC	8	SCL																							
9	HSYNC	10	SDA																							
H4	<p>GPIO1</p> 	<table border="1"> <thead> <tr> <th>Pin</th> <th>Signal</th> <th>Pin</th> <th>Signal</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>GPIO0</td> <td>2</td> <td>+5V</td> </tr> <tr> <td>3</td> <td>GPIO1</td> <td>4</td> <td>GPIO4</td> </tr> <tr> <td>5</td> <td>GPIO2</td> <td>6</td> <td>GPIO5</td> </tr> <tr> <td>7</td> <td>GPIO3</td> <td>8</td> <td>GPIO6</td> </tr> <tr> <td>9</td> <td>GND</td> <td>10</td> <td>GPIO7</td> </tr> </tbody> </table>	Pin	Signal	Pin	Signal	1	GPIO0	2	+5V	3	GPIO1	4	GPIO4	5	GPIO2	6	GPIO5	7	GPIO3	8	GPIO6	9	GND	10	GPIO7
Pin	Signal	Pin	Signal																							
1	GPIO0	2	+5V																							
3	GPIO1	4	GPIO4																							
5	GPIO2	6	GPIO5																							
7	GPIO3	8	GPIO6																							
9	GND	10	GPIO7																							
H5	<p>USB34,USB56</p> 	<table border="1"> <thead> <tr> <th>Pin</th> <th>Description</th> <th>Pin</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>+V5</td> <td>2</td> <td>+V5</td> </tr> <tr> <td>3</td> <td>USB-</td> <td>4</td> <td>USB-</td> </tr> <tr> <td>5</td> <td>USB+</td> <td>6</td> <td>USB+</td> </tr> <tr> <td>7</td> <td>GND</td> <td>8</td> <td>GND</td> </tr> <tr> <td></td> <td></td> <td>10</td> <td>NC</td> </tr> </tbody> </table>	Pin	Description	Pin	Description	1	+V5	2	+V5	3	USB-	4	USB-	5	USB+	6	USB+	7	GND	8	GND			10	NC
Pin	Description	Pin	Description																							
1	+V5	2	+V5																							
3	USB-	4	USB-																							
5	USB+	6	USB+																							
7	GND	8	GND																							
		10	NC																							
H6	<p>CPLD_FH</p> 	<table border="1"> <thead> <tr> <th>Pin</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>+V3.3A</td> </tr> <tr> <td>2</td> <td>CPLD_TDO</td> </tr> <tr> <td>3</td> <td>CPLD_TDI</td> </tr> <tr> <td>4</td> <td>Connect the Cap</td> </tr> <tr> <td>5</td> <td>NC</td> </tr> <tr> <td>6</td> <td>CPLD_TMS</td> </tr> <tr> <td>7</td> <td>GND</td> </tr> <tr> <td>8</td> <td>CPLD_TCK</td> </tr> </tbody> </table>	Pin	Description	1	+V3.3A	2	CPLD_TDO	3	CPLD_TDI	4	Connect the Cap	5	NC	6	CPLD_TMS	7	GND	8	CPLD_TCK						
Pin	Description																									
1	+V3.3A																									
2	CPLD_TDO																									
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4	Connect the Cap																									
5	NC																									
6	CPLD_TMS																									
7	GND																									
8	CPLD_TCK																									

2.3 Jumper Setting and Pin definition

Item	JUMPER NAME	DEFAULT	DESCRIPTION
J1	CLRTC 	1-2	CLR CMOS NORMAL (Default) 2-3 CLR CMOS
J2	GPIOV5 	1-2	GPIO Voltage selection 1-2 +V5 (Default) 2-3 +V3.3
J3	BP_SEL 	2-3	Bypass selection 1-2 Bypass 2-3 NORMAL (Default)
J4	PSON 	2-3	ATX / AT Mode 2-3 AT Mode (Default)